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ANNEALED TEMPERATURE SOL-GEL DEPOSITED P-CHANNEL TYPE $CU_XCR_{1-X}O_{2-\Delta}$ THIN FILM TRANSISTORS

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Abstract:

Thin-film transistors (TFTs) were created in this study by integrating transparent p-type $CuCr_{1-x}Oy$ semiconductor thin films, which were created using spin coating. ($x = 0.0 \le x \le 0.4$)) . For P-type thin-film transistors, which are essential parts of printed electronics, Cu-based films offer a low-cost and low-energy manufacturing method. $CuCr_{1-x}O2$ thin-film device performance was thoroughly examined, along with its structural and morphological elements and optical characteristics. When the annealing temperature (Ta) exceeded 750° C, the phase transition from a combination of CuCr2O4 and CuO to pure CuCrO2 was achieved. The optimized $Cucr_{1-x}o_2$ TFT has a Resistivity Value about 0.021 Ω cm, an on/off current ratio of 10^7 and a hole mobility of 0.61 $cm^2V^{-1}S^{-1}$. The construction and operation of p-Type oxide TFTs are briefly summarized in

this study, along with the challenges and advancements in oxide transistor and CMOS logic circuit development.

Keywords: Oxide Thin-Film transistors, Sol – gel Processed, Resistivity, Mobility

INTRODUCTION: The field of electro-optics has been greatly interested in delafossite semiconductors because of their special qualities and the availability of p-type materials that can be used in solar cells, photo catalysts, photo detectors (PDs), and p-type transparent conductive oxides (TCOs). Due to its superior mobility and reduced leakage current over a-Si TFTs, oxide thin-film transistors (TFTs) are extensively utilized in the display sector. These high-mobility TFTs are needed to enable high-resolution screens for fast driving. Furthermore, by utilising oxide TFTs' low leakage current properties, the power consumption of these displays can be decreased. Applications in industry, science, and technology are seeing a growth in the significance of thin film technology. Complementary circuits that enable low power dissipation and high noise resistance rely heavily on P-type inorganic TFTs. P-type metal oxide semiconductors have been the main focus of current work in the solution processing of the active material for p-type TFTs. In the hottest field of producing extremely effective p-type The general formula for TCOs, copper-based delafossite oxides, is Cu1+M $^{3+}$ O_2 (where M can be any of the following: Al,[5] Fe[6],Ge[7] Ga[8], Cr[9], Y[10] or Sc[11]).promising materials since $CuAlO_2$[5]was initially reported[1-2], which showed good transparency and p-type conductivity. The best p-type TCO among them is copper chromium oxide, or $CuCrO_2$, which has a band gap of about 3.1–3.3 eV_s[12] [3-6]and offers stoichiometric films high electrical resistivity (ρ= 1 Ω cm) and good transparency. Thankfully, oxide TFT devices can overcome the limitations of silicon-based TFTs by using oxide semiconductors as their core material. Nowadays, oxide TFTs, such as wide-bandgap semiconductors or insulators, has good optical transmittance and strong electrical conductivity, making them a feasible substitute. The material's transparency and conductivity are impacted by the bandgap width[7-11], though. Despite their great conductivity, metallic materials are opaque, thus they are not a good substitute. A material with a broad bandgap and strong transparency is likely to have a low carrier concentration, which results in low conductivity. However, a material can only achieve excellent conductivity and transmittance throughout the visible area if its bandgap is larger than 3 eV and its carrier concentration is between 10^{19} and 10^{20} cm−3 [12-16]. There are several methods for creating CuCrO2 films, including sputtering, molecular-beam epitaxy, spray pyrolysis, chemical vapour deposition (CVD)[17-19], sol gel, atomic layer deposition (ALD), hydro-thermal synthesis, and pulsed laser deposition (PLD)[20-23]. Among these, chemical techniques work well with glass and even plastic substrates, allowing for the deposition over vast surface areas at a relatively low temperature (<400 ^{0} C).

Experimental Methods:

Chromium nitrate nonahydrate ($Cr(NO_3)3<9H_2O$, 99.95%, Aladdin) and cupric

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acetate anhydrous ($Cu(COOCH_3)2$, 99.99%, Aladdin) were dissolved to create CuCrxOy precursor solution (0.1 M).in 1-to-1 molar ratio in 2-methoxyethanol ($C3H_8O_2$, 99.9%, Aladdin). A deep green precursor solution that was transparent was formed when the mixture was agitated for five hours at room temperature. The Si wafer, which was heavily doped and had a resistivity of 10^3 O cm, was cleaned with acetone, ethanol, and deionized water in that order before being dried with a nitrogen cannon. The SiO2 layer was 100 nm thick.SiO2/Si substrates were spun with the CuCrxOy precursor solution for 20 seconds at a speed of 5800 rpm. The gel films were annealed for two hours at 450^0 C in air following the coating process.

Results and discussion:

$CuCr_{1-x}Oy$ thin-film structural analysis as a function of annealing temperature was performed and is displayed in Fig. 1a.For the $CuCr_{1-x}Oy$ thin films that were air-annealed at 400 ^{0}C, a weak One may observe the peak of CuO (PDF #45-0937). The thin films that were annealed at 550^0C and 600^0C showed two-phase structures made of CuO (PDF #45-0937) and CuCr2O4 (PDF #34-0424).The phase transition from CuO and CuCr2O4 mixtures to CuCrO2 (PDF #39-0247) happened when the annealing temperature (Ta) was raised to 800 ^{0}C. The following reaction is the basis for the phase transition: $CuO(s) + CuCr_2O_4(s)$ - $2CuCrO_2(s) + 1/2O_2(g)$. Fig. 1b shows the phase transition scheme. This finding suggests that the reduction of Cu^{2+} to Cu^+ is made possible by annealing at 800^0C in a N2 atmosphere. The enhanced film crystallinity is indicated by the reduced whole width at half maximum of the $CuCrO_2$ peaks and the increasing peak intensity with further Ta increase. The devices' carrier transport properties may certainly be enhanced by reducing the grain boundaries, which typically serve as carriers' locations of dispersion and entrapment.

The spectra from XPS studies were used to analyze the phase conversion of $CuCr_{1-x}Oy$ thin films at different temperatures, and they are displayed in Fig. 2 and 3. It's convenient to use XPS. Since the difference in approximately equal to 1 eV is relatively considerable, it is possible to discriminate between the Cu^+- and Cu^{2+}-involved phases by calculating the binding energies of Cu 2p1/2 and Cu 2p3/2.thirty Typical Cu 2p spectra show that Cu occurs in CuCrxOy thin films as the Cu2+ form at Ta as low as 550 and 700^0C. Conversely, the presence of CuO is implied by the satellite peaks, which are seen at 941.6 and 961.9 eV. The Cu 2p1/2 and Cu 2p3/2 peaks move to lower binding as the Ta is raised to 750 1C. The two peaks, which are centered at 931.7 and 932.9 eV and correspond to the Cu+ and Cu2+ cations, are formed by deconvoluting the binding energies of the Cu 2p3/2 peak.

In the CuCrxOy thin films, the ratio of Cu+ / (Cu+ + Cu2+) increases dramatically from 20% to 85% with an increase in Ta from 550^0C to 900^0C. The high-temperature

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annealing process (4800^0C) in a N2 environment is responsible for the phase conversion of CuO and $CuCr_2O_4$ mixes to pure-phase CuCrO2, as evidenced by the XPS results that align with the XRD analysis.

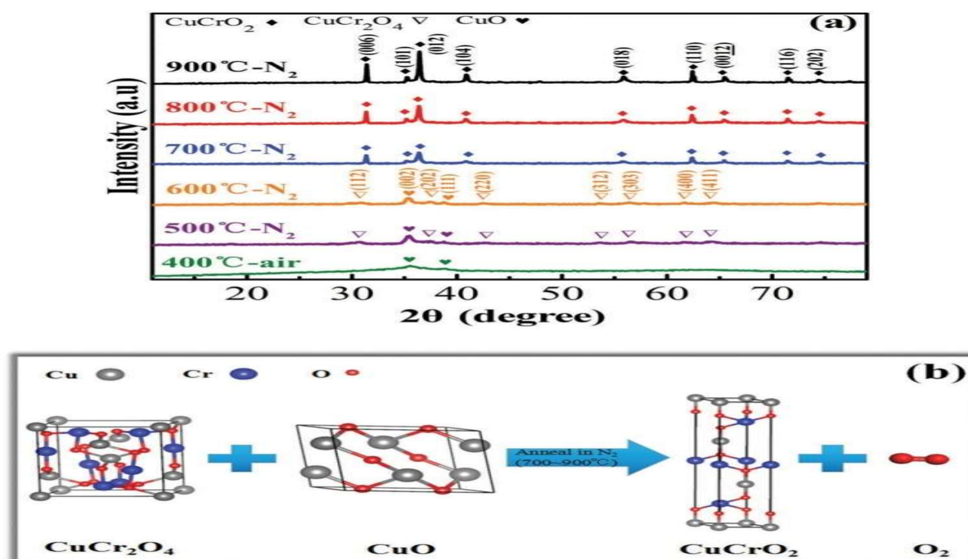

Fig 1 (a) CuCr $_{1-x}$Oy thin film XRD patterns after annealing at different temperatures

(b) Schematic Phase Information of $Cucro_2$

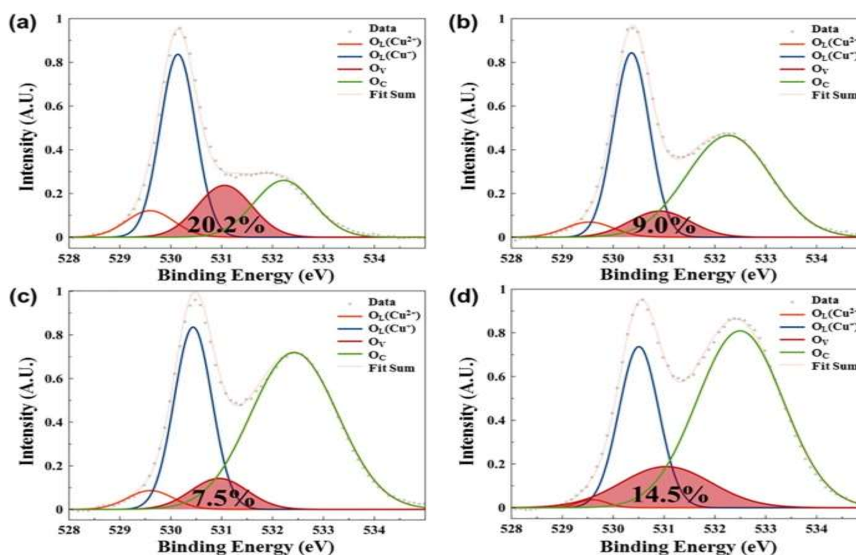

Fig 2: O 1s peak of XPS analysis as Cr doping concentration increased.
(a) Pristine Cu_2O, (b) Cr:Cu_2O #1, (c) Cr:Cu_2O #2, and (d) Cr:Cu_2O #3.

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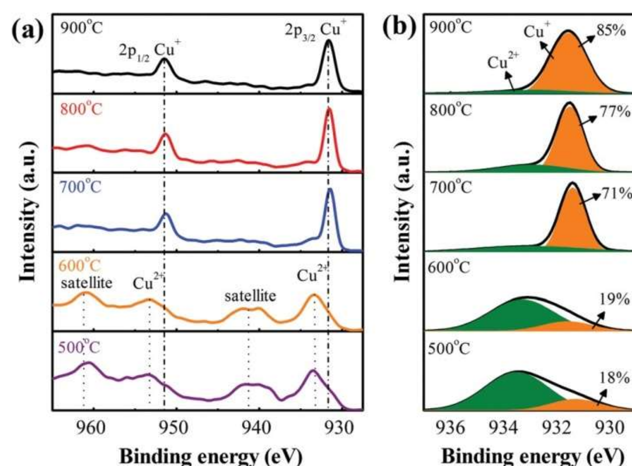
Fig 3: XPS spectra of the $CuCr_{1-x}Oy$ thin films annealed at different temperatures: (a) Cu 2p and (b) Cu 2p3/2



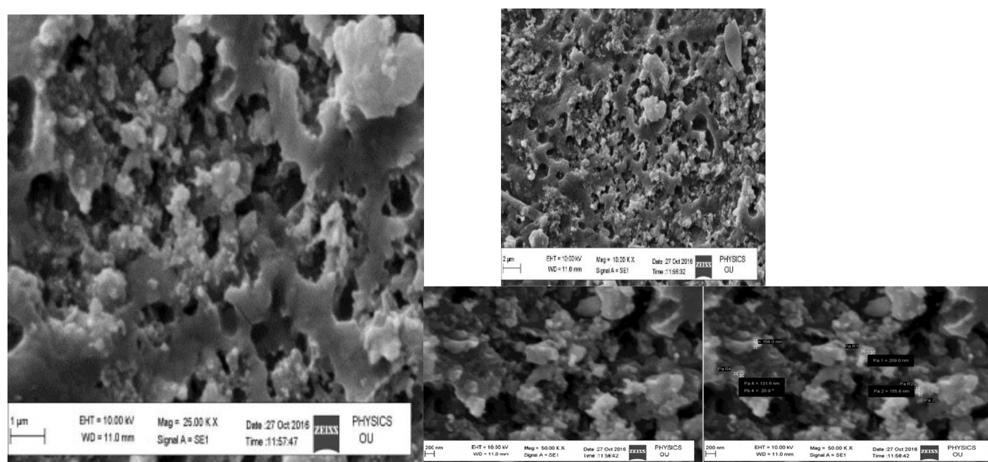


Fig 4: SEM images of the $CuCr_{1-x}Oy$ thin films annealed at (a) 500 ^{0}C, (b) 600 ^{0}C, (c) 700 ^{0}C, and (d) 800 ^{0}C.

Surface morphology is a crucial factor in determining the device performance of TFTs with thin channel layers, as it has a considerable impact on electrical contacts and trap density. $CuCr_{1-x}$ Oy thin film surface morphologies were investigated using SEM, and the resulting pictures are displayed in Fig. 4. After annealing the $CuCr_{1-x}Oy$ thin films at 500, 600, 700, and 800 ^{0}c the corresponding root-mean-square (RMS) values are 5.64, 3.78, 3.57, 2.99, and 2.88 nm. One possible explanation for the lower RMS value at a larger Ta is the rise in surface energy. In this work, the evolution of surface

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morphology is subordinated to the evolution of surface energy. Atoms typically migrate to lower energy sites at high annealing temperatures.

Main Structures of p-Type Oxide Semiconductor TFTs

TFTs are similar to MOSFETs and other field-effect devices in that they are constructed of semi-conductors in the metal insulating layer and have three terminals [24-27]. As seen in Figure, TFTs typically have a stacked structure with the gate and source-drain on opposite sides of the active layer. These structures can be classified into four types based on the positions of the source-drain and gate as well as the bottom gate: bottom-gate-top, bottom-gate-bottom, top-gate-top, and top-gate-bottom contact types as shown in figure 5[28-33]

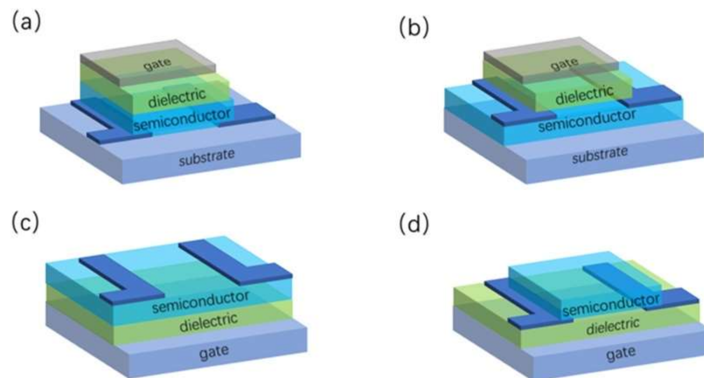

Figure 5: TFT structure, divided by the position of the source-drain and gate: (a) bottom-gate-top contact types; (b) bottom-gate-bottom contact types; (c) top-gate-top contact types; (d) top-gate- bottom contact types

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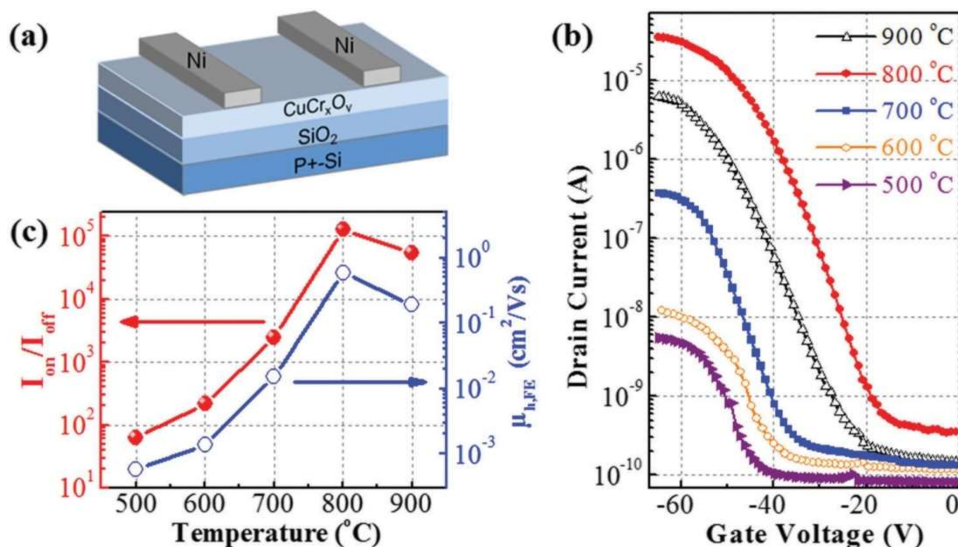

Fig. 6 (a) Schematic diagram of the TFT structure used in this study. 7(b) Transfer characteristics of the $CuCr_xO_y$ TFTs annealed at various temperatures. The variations of I_{on}/I_{off} and $m_{h,FE}$ for the $CuCr_xO_y$ TFTs

Figure 6a shows the construction of bottom-gate and top-contact TFTs on SiO2/p+-Si substrates in order to study the carrier transport parameters of the CuCrxOy thin films. The CuCrxOy TFTs annealed at different temperatures and their transfer characteristics are displayed in Fig. 6b. Figure S2 (ESI) shows the device's gate leakage current curves. Table 1 presents an overview of the important device parameters, such as mh, FE, Ion/Ioff, V_{TH}, and sub threshold swing (SS). It is evident that the CuCrxOy TFTs exhibit p-type conduction behaviour when the drain current (I_{DS}) increases monotonically when the gate voltage (V_{GS}) is lower. When V_{GS} is negative (within the zeroth approximation, r = Ci (V_{GS})), the CuCrxOy/SiO2 interface experiences an increase in carrier concentration, or the field-induced accumulation layer, which may be the cause of the increase in I_{DS}.

It has been noted that as Ta rises from 500 ^{0}C to 800 ^{0}C, both the on-state current (Ion) and the off-state current (Io⇗) increase. This suggests that hole transport has significantly improved at greater Ta. This could be because there are fewer grain boundaries at higher Ta, which leads to better film shape and stoichiometry. Furthermore, the positively increasing V_{TH} suggests a decrease in both the number of grain boundaries in CuCrxOy channel layers and the number of hole traps at the CuCrxOy/SiO_2interface.45 It is well known that induced carriers can only move via a small area close to the channel/dielectric interface. Hole transport and device performance will surely benefit from the reduced quantity of faults.

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When it comes to electrical performance, TFTs annealed at 700 ^{0}C and 800^{0}C outperform those annealed at lower temperatures (i.e., 500 ^{0}C and 600 ^{0}C). It is possible that phase-pure $CuCrO_2$ is formed as a result of the removal of insulator-like $CuCr_2O_4$. With an Ion/Ioff of B10^6 and a high mh, FE of 0.61 cm^2 V^{-1} s^{-1}, the $CuCrO_2$ TFT annealed at 800 ^{0}C shows the best electrical performance. To the best of our knowledge, these prior publications on binary p-type Cu-based oxide TFTs synthesized in the past have a substantially larger mh, FE

able 1. Key electrical Parameters for Various $CuCr_{1\text{-}}xOy$ TFTs

Temperature (^{0}C)	M_h FE (cm^2 $V^{-1}S^{-1}$)	V_{th} (V)	$I_{on/off}$	SS ($Vdec^{-1}$)
500	5.71×10^{-4}	--- 48.07	B51	6.14
600	1.61×10^{-3}	--- 45.76	2.2×10^2	5.96
700	1.54×10^{-2}	--- 43.61	2.1×10^3	5.84
800	0.67	---- 33.82	B 10^6	5.65
900	0.23	---- 41.38	5.1×10^4	6.49

Table2.Transfer Characteristics (Parameter of Five TFTs for each Condition) as Cr Doping Concentration Increased

Sample	Saturation mobility (cm^2/V_s)	V_{th} (V)	$I_{on/off}$	S –factor (v/dec)
Cu_2o	0.47	-8.04	2.72×10^2	12.46
Cr : Cu_2O # 1	0.81	-4.46	1.05×10^3	10.34
Cr : Cu_2O # 2	0.71	-4.48	1.21×10^4	7.68
Cr : Cu_2O # 3	0.32	27.16	1.02×10^2	14.88

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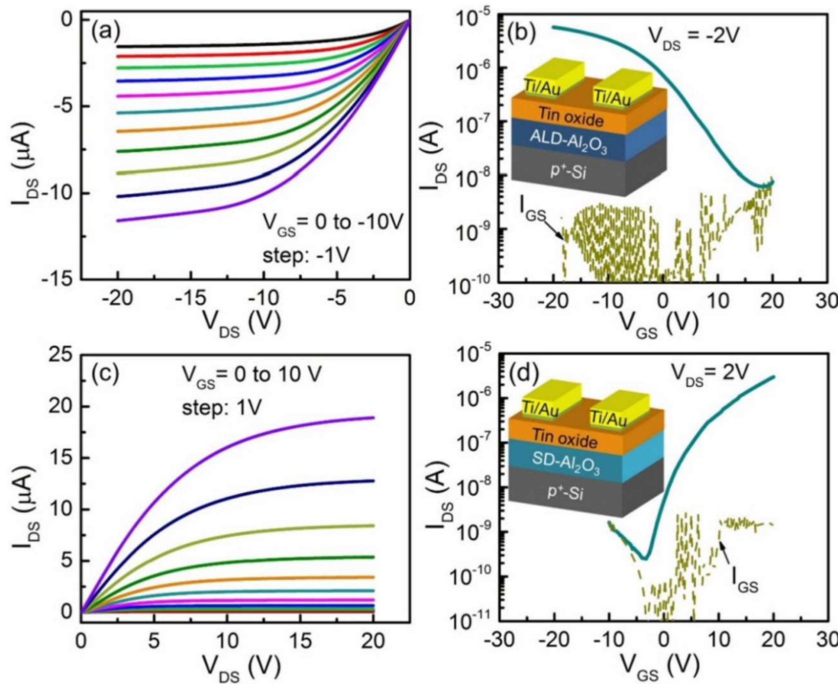
The switching characteristics of pristine Cu_2O TFTs were subpar, exhibiting a saturation mobility (μ_{sat}) of 0.47 cm^2 /Vs, a threshold voltage (Vth) of −8.04 V, an on/off-current ratio (Ion/off) of 2.72×10^2 and an S-factor of 12.46 V/dec.



Performance of n- and p-channel tin oxide TFTs (**a**) Output and (**b**) transfer characteristics of tin oxide p-channel TFTs using ALD-Al_2O_3 as a gate dielectric. (**c**) Output and (**d**) transfer characteristics of tin oxide n-channel TFTs using SD-Al_2O_3 as a gate dielectric

The derivation equation for μ_{sat} is identical to equation (1). By fitting the square root of the transistor's I_{ds} vs Vgs curve linearly in the saturation zone. V_{th} was determined Equation 2 displays the formula used to calculate the S-factor.

$$\mu_{sat} = 2K \ / \ C_{oy} W [\Delta \sqrt{I_{ds}} / \Delta v_{gs}]^2 \qquad \text{---------- (1)}$$

$$S - \text{factor} [\Delta \log (I_{ds}) / \ \Delta V_{gs}] - 1 \qquad \text{----------- (2)}$$

The V_{th} of Cr :Cu_2O #1 and Cr :Cu_2O #2 compared with pristine Cu_2O shifted to positive. The Concentration of Vo Increased from 8.05 to 14.6 as shown in table 2

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Future Challenges:

I. Precision thin-film transistors, which are essential parts of printed electronics, can be cheaply and energy-efficiently fabricated using printing-enabled solution processing of semiconductors, particularly Cu-based films. The current approach is constrained by a discrepancy between printable ink compositions and ink compositions that provide excellent electrical performance at low processing temperatures.

II. For the mass-production of TFTs, particularly those on flexible plastic substrates, the process temperature is crucial. While n-type oxide films can be effectively fabricated using a number of low-temperature techniques, applying these techniques to p-type oxides is still challenging.

III. The vacuum processing method needs to be replaced by continuous processes with better throughput in order to realize revolutionary large-area and cost-effective applications, like foldable and printable screens, disposable smart labels, and smart packaging.

IV. The performance levels of p-type TFT devices are still far from matching those of their n-type counterparts, which are now mass-produced for the display market, despite tremendous advancements in this area. High off-state current, high interfacial defect/states and other critical areas need to be addressed in terms of future research objectives.

Conclusions:

In conclusion, solution-processed CuCrxOy TFTs annealed at different temperatures were integrated for the first time, and p-type ternary CuCrxOy thin films were created utilizing a spin coating technique. As Ta levels rise in a N2 atmosphere, It was possible to obtain phase-pure CuCrO2 at 750^0 C. In the meantime, as Ta increased, so did the film's crystallinity, surface morphology, and transmittance in the visible spectrum. Applications of CuCrxOy thin films as channel layers in bottom-gated TFTs were investigated to examine their electrical performance. High electrical performance is demonstrated by the optimized $CuCrO_2$ TFT.

V_0 typically has an impact on the electrical performance of oxide TFTs. As hole-trapping sites, V_0 interfered with the carrier flow, weakening the electrical properties of p-type oxide TFTs in contrast to n-type oxide TFTs. We verified the performance gains for Cu_2O TFTs without Cr but with an optimized Cr doping concentration, as follows: an S-factor of 7.68 from 12.46 V/dec, an $I_{on}/_{off}$ of 1.21×10^4 from 2.72×10^2, a μ_{sat} of 0.71 from 0.47 cm^2 /V_s, and a V_{th} of −4.48 from −8.04 V. According to these findings, Cr doping increased the hole carrier's conduction mechanism and the TFTs' switching properties.

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